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EFFICIENT AND ENHANCED SHIFT REGISTER DESIGN USING PULSED LATCHES WITH CLOCK GATING TECHNIQUE

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ABSTRACT:

Flip-flops is perilous timing elements in digital circuits which have a huge influence on the circuit speed and power consumption. The performance of flip-flop is an significant element to regulate the efficiency of the entire synchronous circuit. This paper recommends a low-power and area-efficient shift register using pulsed latches. Therefore area and power consumption are reduced by substituting flip-flops with pulsed latches. This technique explains the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals as an alternative of the conventional single pulsed clock signal. Also the shift register uses a small number of the pulsed clock signals by grouping the latches to more than a few sub shifter registers and using supplementary temporary storage latches.

KEYWORDS: flip-flop, Latch, Edge trigger, Level Trigger, Shift Register, pulsed latches, Power optimized.

INTRODUCTION:

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches. This paper proposes a low-power and area-efficient shift register using pulsed latches.

The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size ofCMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers oftransistors onto the same die. The more transistors there will be more switching and more power dissipated in the form ofheat or radiation. Heat is one of the phenomenon packaging challenges in this epoch, it is one of the main challenges oflow power design methodologies and practices. Another driver of low power research is the reliability of the integratedcircuit. More switching implies higher average current is expelled and therefore the probability of reliability issuesoccurring rises. We are moving from laptops to tablets and even smaller computing digital systems. With this profoundtrend continuing and without a match trending in battery life expectancy, the more low

power issues will have to beaddressed. The current trends will eventually mandate low power design automation on a very large scale to match thetrends of power consumption of today's and future integrated chips[3]. Power]consumption of Very Large ScaleIntegrated design is given by generalized relation, P = CV2f [1]. Since power is proportional to the square of the voltageas per the relation, voltage scaling is the most prominent way to reduce power dissipation.

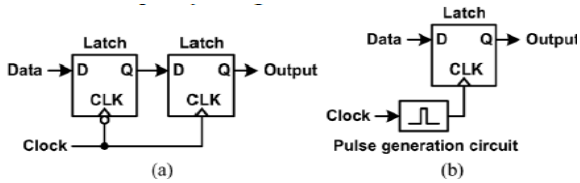
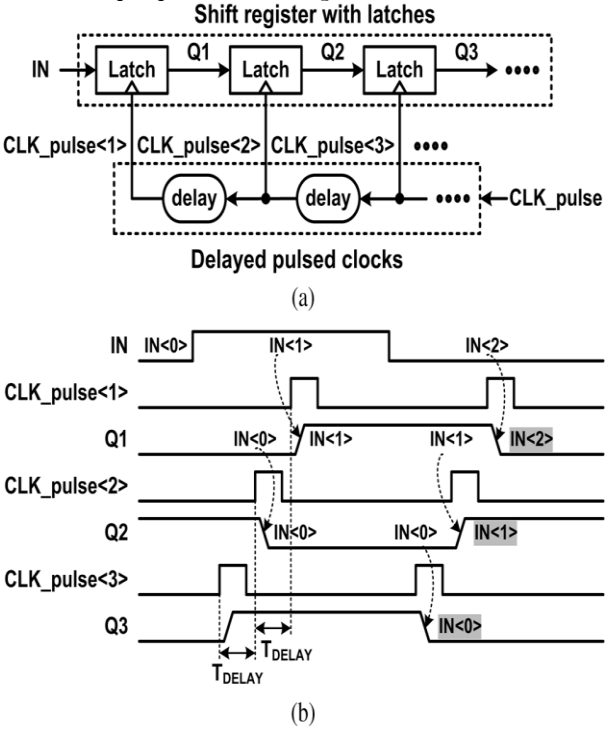
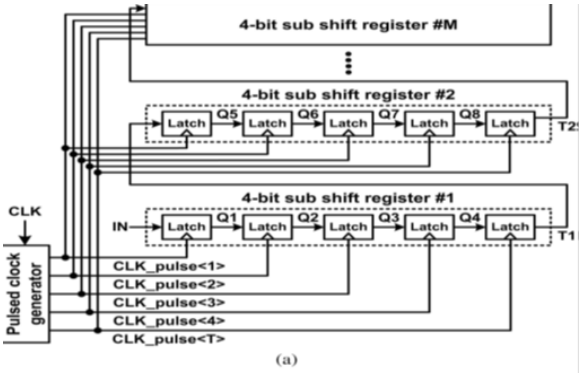


Fig.1. (a) Master-slave flip-flop (b) Pulsed latch

However, voltage scaling isresults in threshold voltage scaling which bows to the exponential increase in leakage power. Though severalcontributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design thatfurther improves the performance of single edge triggered flipflops[2].patterns. The architecture of a shift register is quite simple. An N-bitshift register is composed of series connected N data flip-flops.The speed of the flipflop is less important than the area andpower consumption because there is no circuit between flip-flipsin the shift register.



Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register. The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig. 6 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an shift register is divided into sub shift registers, the number of clock-pulse circuits is and the number of latches is . A sub shift register consisting of latches requires pulsed clock signals. The number of sub shift registers becomes , each sub shift register has a temporary storage latch. Therefore, latches are added for the temporary storage latches. The conventional delayed pulsed clock circuits in Fig. 4 can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals. The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register . is selected by considering the area, power consumption, speed. The area optimization can be performed as follows. When the circuit areas are normalized with a latch, the areas of a latch and a clock-pulse circuit are 1 and , respectively. The total area becomes . The optimal for the minimum area is obtained from the first-order differential equation of the total area . An



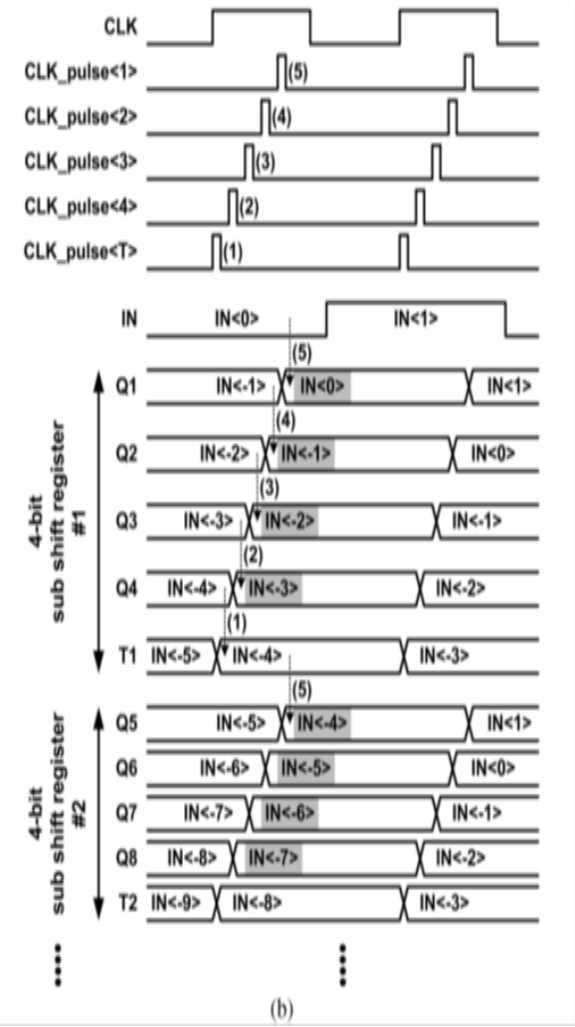


Fig. 5. Proposed shift register. (a) Schematic. (b) Waveforms.

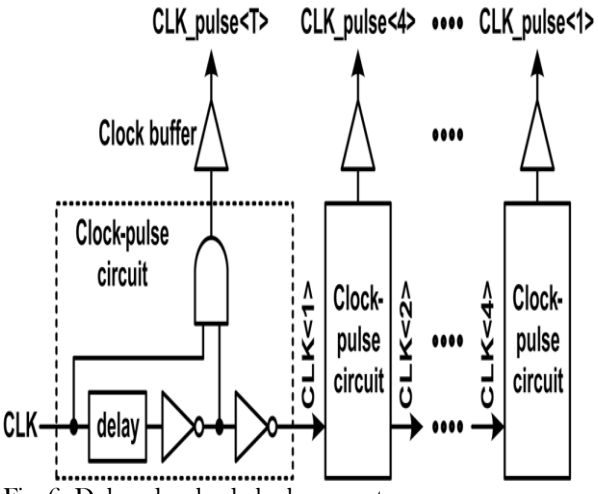


Fig. 6. Delayed pulsed clock generator.

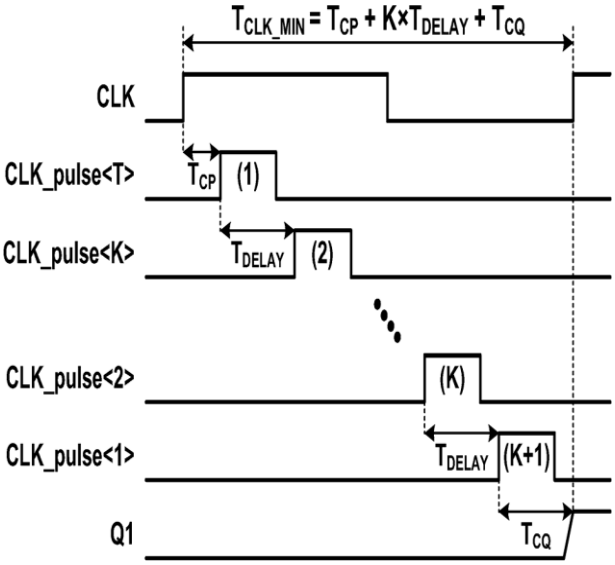
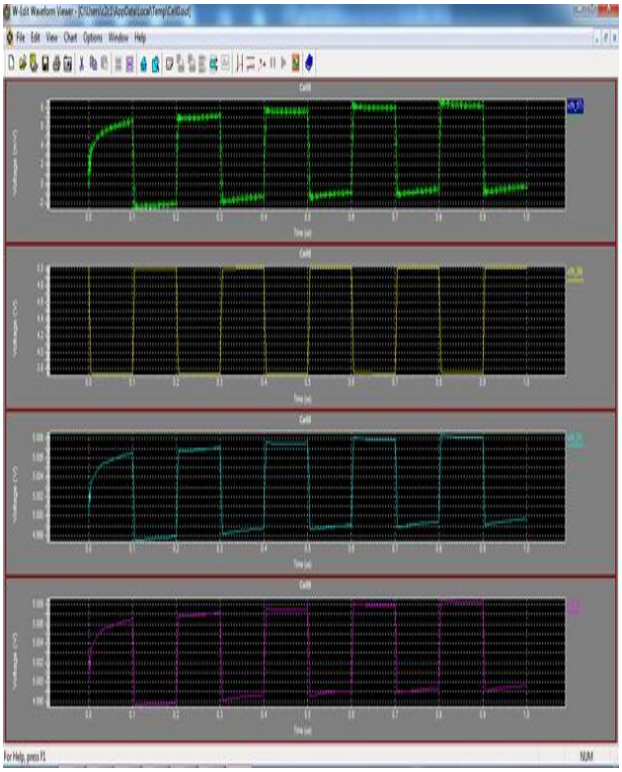


Fig. 7. Minimum clock cycle time of the proposed shift register.

The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are 1 and , respectively. The total power consumption is also . An integer for the minimum power is selected as a divisor of , which is nearest to . In selection, the clock buffers in Fig. 6 are not considered. The total size of the clock buffers is determined by the total clock loading of latches. Although the number of latches increases from to , the increment ratio of the clock buffers is small. The number of clock buffers is . As increases, the size of a clock buffer decreases in proportion to because the number of latches connected to a clock buffer is proportional to . Therefore, the total size of the clock buffers increases slightly with increasing and the effect of the clock buffers can be neglected for choosing . The maximum number of is limited to the target clock frequency. As shown in Fig. 7 the minimum clock cycle time is , where is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal (CLK_pulse1), is the delay of two neighbor pulsed clock signals, is the delay from the rising edge of the last pulsed clock signal (CLK_pulse1) to the output signal of the latch Q1. is proportional to . As increases, the maximum clock frequency decreases in proportion to . Therefore, must be selected under the maximum number which is determined by the maximum clock frequency of the target applications. The pulsed clock signals in Fig. 7 are supplied to all sub shift registers. Each pulsed

clock signal arrives at the sub shift registers at different time due to the pulse skew in the wire. The pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew differences between the different sub shift registers do not cause any timing problem, because two latches connecting two sub shift registers use the first and last pulsed clocks (CLK_pulse[T] and CLK_pulse[1]) which have a long clock pulse interval. In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.

RESULT:



CONCLUSION:

Thus the new design of a static Master-Slave Flipflop based Universal shift register with reduced transistor count renders better efficiency in terms of power and area reduction. The proposed Universal shift register is investigated using the standard parameters, optimization techniques and extensive simulation procedure and the results of the simulation indicate that the proposed design is ideally suited for low power and high performance systems. This paper proposed a low power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches.

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